I. SVX4 ESD Protection

The ESD protection for SVX4 uses both diodes and active clamp circuits to ensure a low impedance conductive path between any two external connections on the chip in case of an ESD discharge through the chip during handling, assembly or installation. Diodes generally implement the conduction between signal pads and supply pads, while the positive supply pads themselves are actively clamped to the substrate for positive-going discharges. The clamp time-constant is ~150 nS (designed for protection against 1.5 kV human body model discharge). Since this period is much shorter that the ramp-up rate of a decoupled system power supply, it should not interfere with normal operation.

A set of figures below depict the ESD protection scheme. Since there are no signal pads that are diode-protected to either the QVDD or SVDD power busses, the supply pads for these busses are missing a low impedance path for negative discharges relative to the substrate. Therefore, bare die could potentially be damaged by such events. This oversight should to be corrected in subsequent versions.

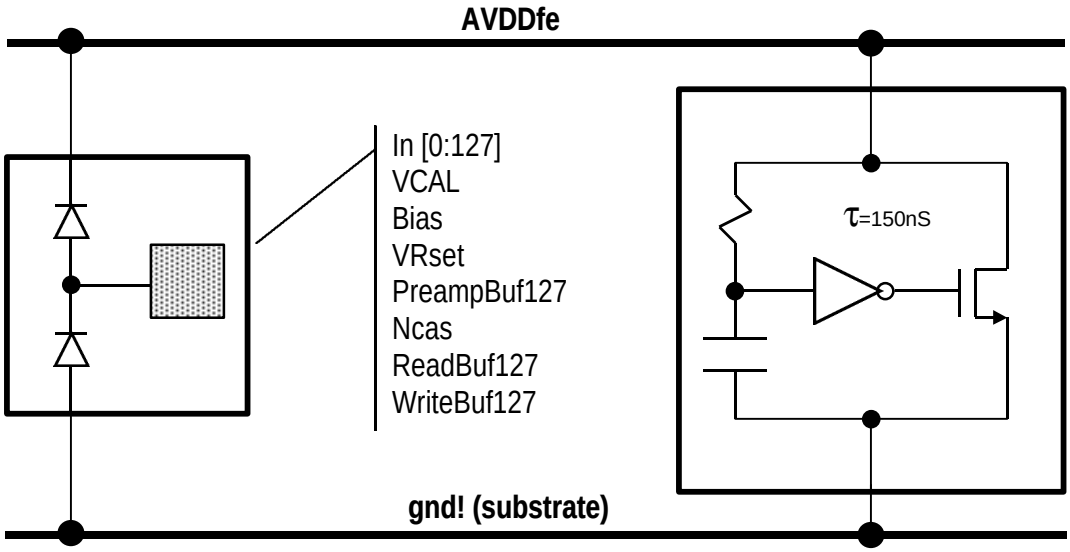

Figure 1: Frontend analog power diagram.

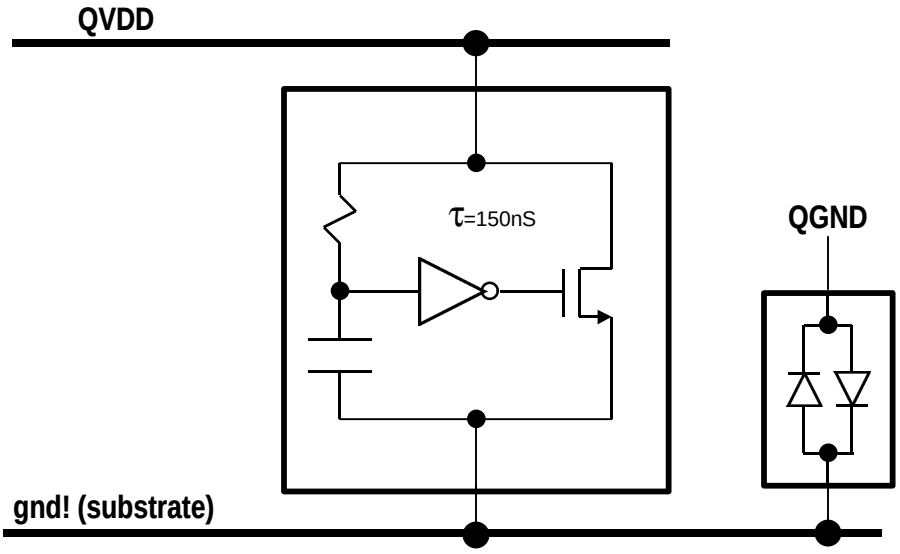

Figure 2: Pipeline QVDD power diagram.

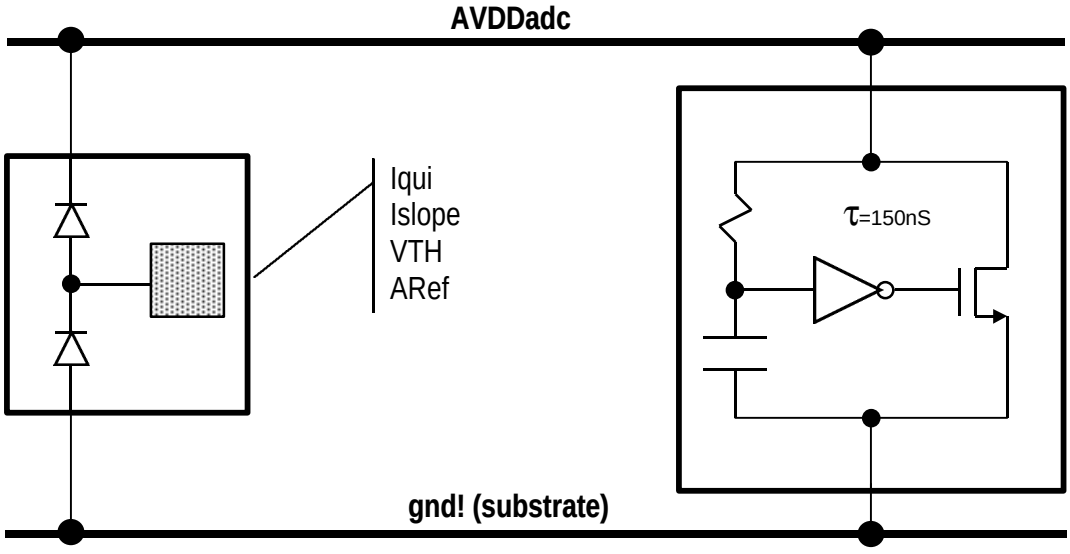

Figure 3: Backend ADC analog power diagram.

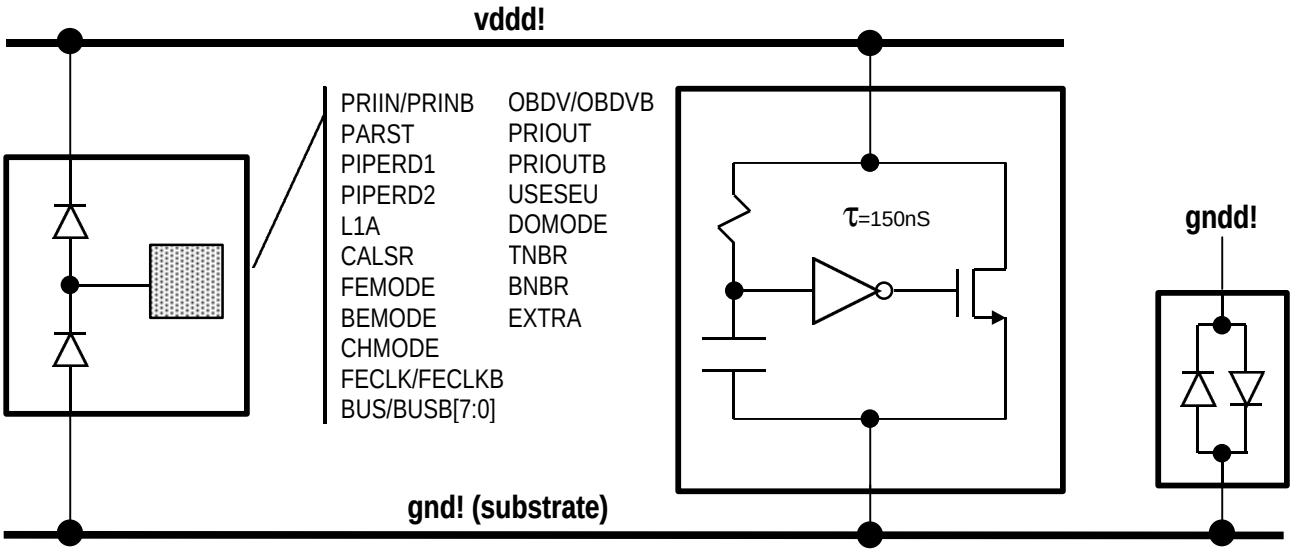

Figure 4: Digital analog power diagram.

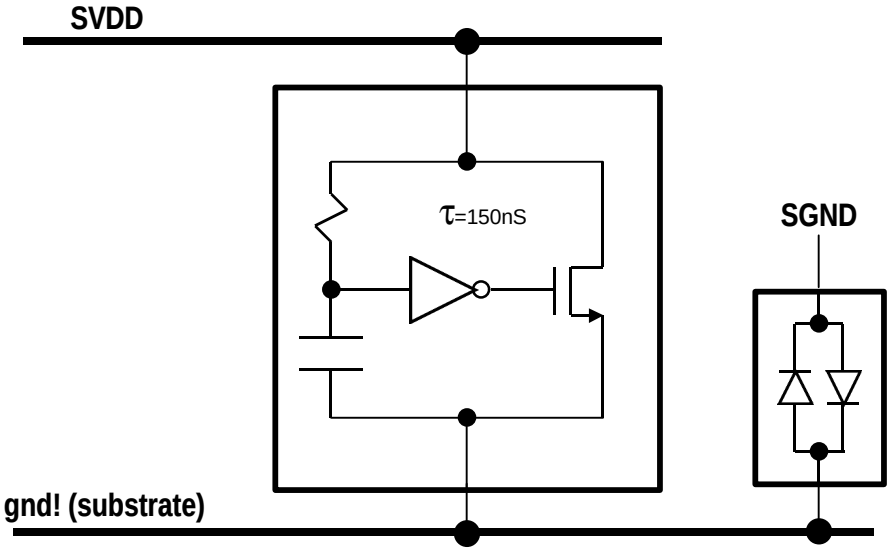

Figure 5: Output driver power diagram.